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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,938	07/10/2003	Eishiro Otani	Q76369	9936

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,938	OTANI ET AL.	
	Examiner	Art Unit	
	William Boddie	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17-36 of

copending Application No. 10/242,666 in view of Tokunaga (US 6,344,715). The following is an example for comparing claim 1 of this application to claim 17 of copending application 10/242,666.

10/615,938 (Claim 1)	10/242,666 (Claim 17)	US 6,344,715
A display device which, according to pixel data for each pixel based on an input image signal, displays an image corresponding to the input image signal (see fig. 1), comprising:	A display device for displaying an image corresponding to an input video signal in accordance with pixel data of each pixel based on said input video signal, comprising:	
A display panel, having a front substrate and rear substrate positioned in opposition such that a discharge space is formed between the front substrate and rear substrate	A display panel having a front substrate and a back substrate opposing each other across a discharge space	
a plurality of row electrode pairs provided	A plurality of row electrode pairs arranged	

on an inner surface of the front substrate such that each row electrode pair defines a display line, and a plurality of column electrodes arranged on an inner surface of the rear substrate such that the plurality of column electrode intersect the plurality of row electrode pairs	on an inner surface of said front substrate, a plurality of column electrodes arranged on an inner surface of said back substrate to intersect with said row electrode pairs,	
and such that a unit light emission area including a first discharge cell and a second discharge cell is formed at each intersecting portion of the plurality of row electrode pairs and the plurality of column electrodes, the second discharge cell	and an unit light emission region formed at each of intersections of said row electrode pairs and said column electrodes and including a first discharge cell and a second discharge cell having a light absorbing layer;	

having a light-absorbing layer and		
A secondary electron emission material layer		17 in fig. 6 and column 7, lines 53-57
Addressing means for applying scan pulses sequentially to one of the row electrodes in each of the row electrode pairs and applying a pixel data pulse derived from the pixel data to each of the column electrodes, for one display line at a time, with the same timing as the scan pulse, to selectively induce address discharge in the second discharge cells, thereby setting the first discharge cells into either a lit state or into an	Addressing means for sequentially applying a scanning pulse to one row electrode of each said row electrode pair while sequentially applying each said column electrode with pixel data pulses corresponding to said pixel data one display line by one display line at the same timing as said scanning pulse to selectively produce an address discharge in said second discharge cell to set said first discharge	

extinguished state; and	cell to one of a lit cell state and an unlit cell state; and	
Sustain means for repeatedly applying a sustain pulse to each of the row electrode pairs to induce sustain discharge only in those of the first discharge cells which are in the lit state.	Sustaining means for repeatedly applying a sustain pulse to each said row electrode pair to produce a sustain discharge only in said first discharge cell set in said lit cell state.	

As can be seen above, claim 17 of copending application 10/242,666 differs from claim 1 of the application in not having a secondary electron emission layer. However, Tokunaga teaches a display device having a secondary electron emission material later (17 in fig. 6).

Therefore, at the time of the applicant's invention it would have been obvious to a person of ordinary skill in the art to include a secondary electron emission material layer in the currently pending application. The motivation for doing so would have been to improve the priming effect further (Tokunaga, col. 8, lines 3-4).

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9-12,15-21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Tokunaga et al. (US 6,344,715).

With respect to claim 1, Tokunaga discloses, a display device which, according to pixel data for each pixel based on an input image signal, displays an image corresponding to the input image signal (see fig. 1), comprising:

A display panel, having a front substrate (202 in fig. 6) and rear substrate (201 in fig. 6) positioned in opposition such that a discharge space (S in fig. 6) is formed between the front substrate and rear substrate, a plurality of row electrode pairs provided on an inner surface of the front substrate such that each row electrode pair defines a display line (X and Y in fig. 5), and a plurality of column electrodes arranged on an inner surface of the rear substrate such that the plurality of column electrode intersect the plurality of row electrode pairs (D1-Dm in fig. 2, and D in fig. 3) and such that a unit light emission area including a first discharge cell (S in fig. 6) and a second discharge cell (SL in fig. 6) is formed at each intersecting portion of the plurality of row electrode pairs and the plurality of column electrodes, the second discharge cell having a light-absorbing layer (30 in fig. 6) and a secondary electron emission material layer (17 in fig. 6);

Addressing means for applying scan pulses sequentially to one of the row electrodes in each of the row electrode pairs (7 and 8 in fig. 2) and applying a pixel data pulse derived from the pixel data to each of the column electrodes (6 in fig. 2), for one display line at a time, with the same timing as the scan pulse (fig. 4), to selectively induce address discharge in the second discharge cells, thereby setting the first discharge cells into either a lit state or into an extinguished state; and

Sustain means for repeatedly applying a sustain pulse to each of the row electrode pairs to induce sustain discharge only in those of the first discharge cells which are in the lit state (see fig. 4 and col. 4, lines 9-26).

With respect to claim 2, Tokunaga discloses, the display device according to claim 1 (see above), wherein the light-absorbing layer is formed on or near the front substrate within each of the second discharge cells (30 in fig. 6), and the secondary electron emission material layer is formed on or near the rear substrate (17 in fig. 6) within each of the second discharge cells.

With respect to claim 3, Tokunaga discloses, the display device according to claim 1 (see above), wherein a fluorescent layer (16 in fig. 6) is formed only within each of the first discharge cells (S in fig. 6).

With respect to claim 4, the display device according to claim 1 (see above), wherein each of the row electrodes in each row electrode pair comprises a main electrode portion extending in a display line direction, and a plurality of electrode tips protruding from the main electrode portion toward the opposite row electrode in the same row electrode pair such that each electrode tip is opposed

to a mating electrode tip, the electrode tips protruding from intersecting portions of the main electrode portion and the column electrodes;

Each of the first discharge cells comprises two mating electrode tips belonging to one row electrode pair; and each of the second discharge cells comprises the main portion of one row electrode in the one row electrode pair and another main portion of a row electrode in a next row electrode pair. (See figures 5-7, the described structure of claim 4, is shown in these figures. These figures illustrate the same row electrode structure as the applicant's shown in figures 6-8)

With respect to claim 5, Tokunaga discloses, the display device according to claim 1 (see above) further comprising reset means for applying a reset pulse (RP in fig. 4) to the row electrodes prior to the address discharge (Wc in fig. 4) caused by the addressing means, to induce reset discharge across the column electrode and the row electrode in each second discharge cell. (also note col. 8, lines 8-10)

With respect to claim 6, Tokunaga discloses, the display device according to claim 1 (see above), further comprising reset means for, prior to the address discharge by the addressing means (see claim 5), applying a positive-polarity reset pulse (RPy in fig. 4) to one row electrode of each of the row electrode pairs and applying a negative-polarity reset pulse (RPx in fig. 4) to the other row electrode of each of the row electrode pairs, to induce reset discharge across the column electrodes and the row electrodes within the second discharge cells as well as within the first discharge cells.

With respect to claim 9, Tokunaga discloses, the display device according to claim 1, further comprising erase means (8 in fig. 2) for inducing erase discharge within the first discharge cells and the second discharge cells by applying an erase pulse (EP in fig. 4) to the row electrodes after the end of the sustain discharge induced by the sustain means (col. 4, lines 62-65).

With respect to claim 10, claim 10 is merely a method claim with the limitations of claim 1. As Tokunaga discloses the method of claim 1, claim 10 is rejected on the same merits as shown above in claim 1.

With respect to claims 11-15, these claims recite identical limitations to claims 5-9 respectively. Thus claims 11-15 are rejected on the same merits as shown above in claims 5-9.

With respect to claim 16, claim 16 is merely an apparatus claim with the same limitations as claim 1. As Tokunaga discloses the apparatus of claim 1, claim 16 is rejected on the same merits as shown above in claim 1.

With respect to claim 17-24, these claims recite identical limitations to claims 2-9. Thus claims 17-24 are rejected on the same merits as shown above in claims 5-9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8,13-14, and 22-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Tokunaga in view of Setoguchi et al. (US 2002/0050960).

With respect to claim 7, Tokunaga discloses, the display device according to claim 6 (see above).

Tokunaga does not expressly disclose, wherein the reset means executes the reset discharge induced in the first discharge cells and the second discharge cells of odd-numbered display lines separated by a time interval from the reset discharge induced in the first discharge cells and the second discharge cells of even-numbered display lines.

Setoguchi discloses, a reset discharge (X electrode reset period in fig. 6) induced in the first discharge cells and the second discharge cells of odd-numbered display lines (x1, x2, x3... in fig. 1) separated by a time interval from the reset discharge (Y electrode reset period in fig. 6) induced in the first discharge cells and the second discharge cells of even-numbered display lines (y1, y2, y3... in fig. 1).

Setoguchi and Tokunaga are analogous art because they are from the same field of endeavor namely, plasma display driver design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to reset the even and odd display lines at different times.

The motivation for doing so would have been to allow for interlaced scanning (Setoguchi, paragraph 46).

Therefore it would have been obvious to combine Setoguchi with Tokunaga for the benefit of interlaced scanning to obtain the invention as specified in claim 7.

With respect to claim 8, Tokunaga discloses, the display device of claim 1 (see above), wherein the reset pulse has a waveform a level transition of which during a rising interval is gradual compared with the sustain pulse. (note the rising gradual pulse shape of RPx and RPy in fig. 4 as compared with SP (sustain pulse) also in fig. 4)

Tokunaga does not expressly disclose, wherein the reset pulse has a gradual falling level transition interval as compared with the sustain pulse.

Setoguchi discloses, a reset pulse with a gradual falling level transition interval (Y electrode reset period in fig. 6) as compared with the sustain pulse (sustain period in fig. 6).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make both the rising and falling transition of the reset pulse gradual.

The motivation for doing so would have been to allow the wall charges to be adjusted arbitrarily by the voltage between the X electrode and Y electrode (Setoguchi, paragraph 41, last sentence).

Therefore, it would have been obvious to combine Setoguchi with Tokunaga for the benefit of arbitrarily adjusting the voltage between the X and Y electrodes to obtain the invention as specified in claim 8.

With respect to claims 13-14 and 22-23, these claims recite the same limitations as shown above in claims 7-8 respectively. Therefore claims 13-14 and 22-23 are rejected on the same merits as shown above in claims 7-8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 8:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

REGINA LIANG
PRIMARY EXAMINER

Wlb
9-6-05